REMARKS

This application has been reviewed in light of the Office Action dated June 17, 2003. Claims 17 and 18 are pending in this application. Claim 17, which is in independent form, has been amended to define more clearly what Applicant regards as his invention, in terms that distinguish over the art of record. Favorable reconsideration is requested.

The Examiner objected to Claim 17 as to an informality in the claim language. In response, Applicant has changed "said first FIFO" to read –said first FIFO section–, as recommended by the Examiner.

The Examiner objected to the drawings, requesting that Figure 2 be labeled "PRIOR ART" and that reference "MUX 9" should read –DEMUX–. In addition, in regard to the latter point, the Examiner also objected to the specification, asserting that "multiplexer 9" at page 1, lines 18 and 23 should read –demultiplexer 9–. Applicant encloses hereto a replacement sheet for Figure 2, which labels Figure 2 –PRIOR ART–. However, Applicant submits that the devices 9 and 10 shown in Figure 2 represent switches that can perform either a switching output or a switching input, and therefore, are suitably referred to as a multiplexer. Applicant submits that the objections to the drawings are specification have been overcome and therefore, respectfully requests their withdrawal.

The Office Action rejected Claim 17 under 35 U.S.C. § 112, second paragraph, as indefinite, asserting that the values of "a" and "n" are not defined. As shown above, Applicant has amended Claim 17 to recite that "a" is a natural number representing a size of the inputted bit width and "n" is a natural number. Applicant submits that the Section 112 rejection has been overcome and therefore respectfully requests its withdrawal.

The Office Action rejected Claims 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,900,857 (Kuwata et al.) in view of U.S. Patent No. 4,745,485 (Iwasaki). Applicant respectfully traverses this rejection.

Applicant submits that amended independent Claim 17, together with Claim 18 depending therefrom, are patentably distinct from the proposed combination of the cited prior art at least for the following reasons.

The aspect of the present invention set forth in Claim 17 is a memory controller comprising a converter section, a first FIFO (first-in-first-out) section, a frame memory section, and a second FIFO section. The converter section performs serial/parallel conversion of image data of "a" bit width inputted into image data of "a" x "2n"-bit width, where "a" is a natural number representing a size of the inputted bit width and "n" is a natural number. The first FIFO section temporarily stores the image data of "a" x "2n"-bit width. The frame memory section stores image data of one frame and a second FIFO section temporarily stores image data read out from the frame memory section.

The image data is read out from the first FIFO section, written into the frame memory section, and read out from the frame memory section, at a rate that is half of a rate at which the image data is inputted into the first FIFO section. In addition, the first FIFO section is of a size suitable for storing image data, so that, within a period for inputting the image data into the first FIFO section to FULL capacity, writing the image data into the frame memory section, a plural times of reading the image data from the frame memory section, and executing a command of the frame memory section are conducted.

Important features of Claim 17 are reading the image data from the first FIFO section at a rate that is half of the rate at which image data is inputted into the first FIFO section, and the FIFO section is of a size suitable for storing the image data, so that, within a period for inputting the image data into the first FIFO section to full capacity, the command of the frame memory section is executed.

Kuwata et al., as understood by Applicant, relates to method of driving a liquid crystal display device and a driving circuit for the liquid crystal display device. The Office Action states (and Applicant agrees) that Kuwata et al. "fail[s] to teach serial/parallel conversion." The Office Action also states that Kuwata et al. teaches "a memory controller comprising a first FIFO section 2, a frame memory section 3, a second FIFO section 5, the timing control section 9 controls the image data RGB (6) is read out from the first FIFO section 2, and read out from the frame memory section 3 at a rate that is half of a rate at which the image data RGB (6) is inputted into the first FIFO section 2, the memory control section 4 controls writing into the frame memory section 3" and asserts that the specification in Kuwata et al. at column 11, lines 44-67, provides support for this assertion. Applicant submits that column 11, lines 44-67, of the specification relates to inputting image data into a frame modulation circuit for each pixel, outputting the image data, temporarily storing the data, and then writing the data based on instructions from a memory control section. Applicant submits, however, that nothing has been found in this section, or any other section of Kuwata et al., that would teach or suggest reading the image data from the first FIFO section at a rate that is half of the rate at which image data is inputted into the first FIFO section, where the FIFO section is of a size suitable for storing the image data, so that, within a period for inputting the image data into the first

FIFO section to full capacity, the command of the frame memory section is executed, as recited in Claim 17.

Iwasaki, as understood by Applicant, relates to a picture display device. The Office Action states that Iwasaki teaches a memory controller which includes a serial/parallel converter.

Accordingly, Applicant submits that even if Iwasaki taught or suggested such a serial/parallel converter, Applicant submits that the proposed combination of Kuwata et al. and Iwasaki, assuming such combination would even be permissible, would still fail to teach or suggest reading the image data from the first FIFO section at a rate that is half of the rate at which image data is inputted into the first FIFO section, and the FIFO section being of a size suitable for storing the image data, so that, within a period for inputting the image data into the first FIFO section to full capacity, the command of the frame memory section is executed, as recited in Claim 17.

Accordingly, Applicant submits that at least for these reasons, Claim 17 is patentable over these two patents, taken separately or in any proper combination.

Claim 18 depends from Claim 17 and, therefore, is submitted to be patentable for at least the same reasons. Since Claim 18 is also deemed to define an additional aspect of the invention, individual reconsideration of the patentability of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

Peter C. Hughes

Attorney for Applicant

Registration No. 47,138.

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200

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